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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/052,338	01/23/2002	Yoshiyuki Imanaka	03500.013949.1	8506

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EXAMINER
DUDDING, ALFRED E

ART UNIT	PAPER NUMBER
2853	

DATE MAILED: 09/30/2002

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/052,338	IMANAKA ET AL.	
	Examiner	Art Unit	
	Alfred E. Dudding	2853	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *31-67* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *31,33,36-51,53,55,57 and 59-67* is/are rejected.

7)☒ Claim(s) *32,34,35,52,54,56 and 58* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on *23 January 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *09/426,896* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892) (7)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 7 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Priority

1. Applicant cannot rely upon the foreign priority papers to overcome this rejection because a translation of said papers has not been made of record in accordance with 37 CFR 1.55. See MPEP § 201.15.

Specification

2. The disclosure is objected to because of the following informalities: *page 23, line13, change ''1441" to - -441- -.

Appropriate correction is required.

Drawings

3. The drawings are objected to because Figure 2, reference character '30' should be '305'. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not

commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 31, 36, 40/31-34, 41 – 43, 47 – 51, 53, 55, 57, 59 - 62, and 65 - 67 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barbour et al. (U.S. 6,315,828 B1) in view of Knothe et al. (U.S. 4,811,293 A).

Barbour et al. discloses a head substrate of a printing head detachably mounted on a printer main body, Figure 1B, element 116 (printhead assembly) and Figure 2, element 236 (printhead cartridge), comprising: plural external connection terminals for externally entering various signals and a driving electric power; Figure 4, elements 406 (contact pads), recording execution means for executing a recording operation according to the various signals and the driving electric power externally entered into said external connection terminals, Figure 1B, element 124 (driver processor) and element 144 (driver head); data memory means for executing data writing and data readout; memory access means for executing the data writing into said data memory means in response to the various signals and the driving electric power externally entered into said external connection terminals and the data readout corresponding to the various signals, Figure 1B: element 122 (memory) is controlled by element 110 (controller) and can communicate also with the processing driver head, Column 4, lines 41 – 42, Column 5, lines12 – 15.

Barbour et al. fail to teach the claimed invention of a writing inhibition means for permanently disabling the data writing into said data memory means by said memory access means.

Knothe et al. discloses a memory device that has write enable protection and permanent disabling of the write enable line, Column 2, lines 41 – 63, Figure 1, element 5, by removing element 5 (switch). Knothe et al. discloses that the switch may be in the form of a jumper wire, Column 2, lines 63 – 68. An examination of the logic diagram of Figure 1 shows that the binary state of the write protect signal and the VDD signal determines if the memory is written or read0only

It would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute the memory of Knothe et al. in the invention of Barbour et al. in order to write protect important data of a device connected to as microprocessor. The motivation/suggestion is given by the '203 patent, Column 1, lines 6 – 27, to protect important stored data upon powering up the microprocessor.

7. Claims 33, 39, and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barbour et al. as applied to claim 1 above, in view of Knothe et al., and further in view of Barbehenn et al. (U.S. 5,363,134 A).

The combination of Barbour et al. and Knothe et al. fail to teach the claimed invention of a writing inhibition means for permanently disabling the data writing into said data memory means by said memory access means.

Barbehenn et al. discloses that the driving signals going to the printhead are in common with the recording circuitry, Figure 5, element 44, and with the memory, element 45.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the wiring of Barbehenn et al, in the combined invention of Barbour et al. and Knothe et al. in order to minimize I/O connections to the printhead. The motivation/suggestion is given by the '134 patent, to minimize or eliminate additional interconnect pads on the printhead, Column 2, lines14 – 18.

8. Claims 37, 63, and 44 are is rejected under 35 U.S.C. 103(a) as being unpatentable over Barbour et al. as applied to claim 1 above, in view of Knothe et al., and further in view of Imanaka et al. (U.S. 6,168,251 B1).

The combination of Barbour et al. and Knothe et al. fail to teach the claimed invention of a memory device with a serial input.

Imanaka et al., discloses a serial input shift register, Figure 5, element 704.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the shift register if Imanaka et al. in the combined invention of Barbour et al. and Knothe et al. in order to minimize I/O wiring to the printhead and in the printhead substrate. The motivation/suggestion is given by the

'251 patent, Figure 5, which shows that element 704 has only three inputs: a shift clock (CLK), a reset (RST), and a data input (DATA).

9. Claims 38, 64, and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barbour et al. as applied to claim 1 above, in view of Knothe et al., and further in view of National Semiconductor, Corp., 1981 Logic Databook, 1981, pp.6-98-101.

The combination of Barbour et al. and Knothe et al. fail to teach the claimed invention of a memory device having a parallel input and a serial output.

National Semiconductor Corp. discloses a serial input shift register having parallel outputs, pages 6-98-101, device DM74LS165.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the National Semiconductor Corp. shift register in the combined invention of Barbour et al. and Knothe et al. in order to accommodate a parallel input from a controller. The motivation/suggestion would be to increase data transfer by transferring n-bits of data with a single clocking pulse as compared to a serial input shift register which requires n clocks to input n-bits of data.

Allowable Subject Matter

10. Claims 32, 34, 35/31-34, 52, 54/51-53, 56, and 58/55-57, are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

a. A search of prior art did not cite a printhead substrate wherein a writing inhibition means is adapted for cutting off an electric power wiring for supplying the driving electric power for data writing from the external connection terminal to said memory access means as claimed in the limitations of claims 32, 34, 52, and 56.

b. A search of the prior art did not cite a method for producing the head substrate wherein the data

writing step writes data of plural kinds in succession in the data memory means by the memory access means; and the writing inhibition step individually disables data overwriting for the data of the plural kinds written in succession in the data memory means by the memory access means, as claimed in the limitations of claims 35/31-34, 54/51-53, and 58/55-57.

Conclusion

11. Reference **JP 08-177732** could not be found on data bases available to the examiner and was not submitted with application **09/436,896**. For this reference to be considered, please submit a copy with the response to this office action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alfred Dudding whose telephone number is (703) 308-6082. The examiner can normally be reached on Monday-Friday from 9:30 AM to 6:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow Jr., AU 2853, can be reached at (703) 308-3126. The fax phone numbers for this Group are (703) 305-3432, (703) 305-3431, (703) 308-7382, (703) 308-7724, and (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the group receptionist whose telephone number is (703) 308-0956.

Alfred Dudding

9-19-02.

John Barlow
Supervisory Patent Examiner
Technology Center 2800